prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides and an amount of overlap between the sides of the gate and a pair of source/drain regions; and

oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

3. (Amended) The method of claim 2, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

4. (Amended) The method of claim 2, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

7. (Amended) A method of forming a transistor, comprising:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate after all source/drain regions have been formed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

9. (Amended) The method of claim 8, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

10. (Amended) The method of claim 8, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

14. (Amended) A method of forming a transistor, comprising:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a nitride layer to the gate dielectric layer, wherein the nitride layer prevents oxide undergrowth;

forming a gate on top of the nitride layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate <u>after all source/drain regions have been formed,</u> wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

16. (Amended) The method of claim 15, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

17. (Amended) The method of claim 15, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

21. (Amended) A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate after all source/drain regions have been formed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and

electrically connecting the number of transistors.

23. (Amended) The method of claim 22, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

24. (Amended) The method of claim 22, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

27. (Amended) A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a first source/drain extension adjacent the first source/drain

region and a second source/drain extension adjacent the second source/drain region;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate after all source/drain regions have been formed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and

electrically connecting the number of transistors.

28. (Amended) A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a nitride layer to the gate dielectric layer, wherein the nitride layer prevents oxide undergrowth;

forming a gate on top of the nitride layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate after all source/drain regions have been formed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and

electrically connecting the number of transistors.

30. (Amended) The method of claim 29, wherein coupling a silicon nitride (SiN) layer to the gate dieiectric layer comprises remote plasma nitride processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

31. (Amended) The method of claim 29, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

35. (Amended) A method of forming a memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate <u>after all source/drain regions have been formed,</u> wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors; and

forming a number of [wordlines] <u>bitlines</u> coupled to the first source/drain region of the number of transistors.

37. (Amended) The method of claim 36, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

38. (Amended) The method of claim 36, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

41. (Amended) A method of forming a memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source drain region in the semiconductor substrate;

forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate <u>after all source/drain regions have been formed,</u> wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors; and

forming a number of [wordlines] <u>bitlines</u> coupled to the first source/drain region of the number of transistors.

42. (Amended) A method of making an information handling system, comprising:

providing a processor chip;

forming a semiconductor memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate after all source/drain regions have been formed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors;

forming a number of [wordlines] bitlines coupled to the first source/drain region of the number of transistors; and

coupling the processor chip to the semiconductor memory device with a system bus.

44. (Amended) The method of claim 43, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

45. (Amended) The method of claim 43, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing [the gate dielectric layer] to form a silicon nitride (SiN) layer.

54. (Amended) A transistor formed by the following process:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate after all source/drain regions have been formed, wherein a portion of